

A study on application of SFCL in vietnam power distribution system with distributed generators (DGs)

Hung Chi Nguyen, Phuc Huu Nguyen

Department of Electrical Electronics and Telecommunications, Saigon University, Vietnam

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ABSTRACT

As the power load demand is rapidly increasing nowadays, many new power generation units are continuously connected to the power system such as small hydropower, wind power, solar cell, and so on. However, in a distribution system, the presence of Distributed Generators (DGs) would generally change the distribution system's behavior. This change can affect to the operation and protection of devices in power system and the original parameters will be deviated. Especially, the fault current of power system with DGs is dramatically increasing, and Superconducting Fault Current Limiter (SFCL) has attracted lots of attention as one of the best correctives to solve these issues. This paper proposes a strategy on application of SFCL in distribution system to solve the problems related to excessive short-circuit current and the mitigation of voltage sag due to the introduction of the DGs. Firstly, a Resistive-type SFCL (R_SFCL) is modeled by Matlab/Simulink. Next, a distribution system of Southern Vietnam power system is selected and simulated. Finally, according to the simulation results, the short circuit current and voltage sag improvements can be validated.

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Corresponding Author:

Hung Chi Nguyen,
Department of Electrical Electronics and Telecommunications,
Saigon University,
No. 273 An Duong Vuong Street, Ward 3, District 5, Hochiminh City, Vietnam.
Email: ngchihung78@gmail.com

1. INTRODUCTION

Due to the rapid growth of load demand, different power sources of green house gases renewable energy (RES) such as photovoltaic (PV) wind power, bio fuel and bio mass are have added to the power system, and the interconnection among various power devices for a modern electric grid also becomes more and more complicated. In addition, conventional power system is facing problems with the fuel resources depletion, as well as environment pollution. Distributed energy sources and the corresponding Distributed Generators (DGs) technology are rising to solve related problems. In terms of the demands, the DGs integration technology has been rapidly developed, such as wind turbines, PV cells, so on [1-3]. Therefore, when the electric system have many DGs installed in to the power system with larger capacity will be increase the short-circuit current if have a fault current occurred it will make reduced the protection characteristics of devices and the lessening of power quality in electric system [4-6]. To preparing for the perversion, there are a lot of high technical problems such as open loop, changing the system structure, replaced and maintained of the breakers, however, the SFCL has recently been taken into consideration [7-10].

SFCL is innovative electric equipment base on the principle of superconductivity. SFCL is an attractive device that limits the short circuit rapidly and effectively without affecting the power system during normal operation. So there are many studies on application of SFCL to electric systems, and various type of SFCLs are implemented at substation of power distribution system in real world power grids of many countries [11-14].

Today, power quality problem is one of the important issues in power system. One of the most significant issues regarding power quality is voltage sag [15]. Voltage sags (drops) are incidents in which the voltage amplitude drops for short time. The voltage sag is indicative of power quality degradation and is a useful measure of the fault event. Nevertheless, there is little progress in the studies on the impact of SFCL's application in improving voltage sags of a distribution system with DGs. In this paper, we have investigated the fault current limiter and evaluated the effects of SFCL in a distribution system with DGs of 22 kV Vietnam power system. The distribution system model using actual data from Moc-Hoa Long-An substation, Vietnam is shown in Figure 1.

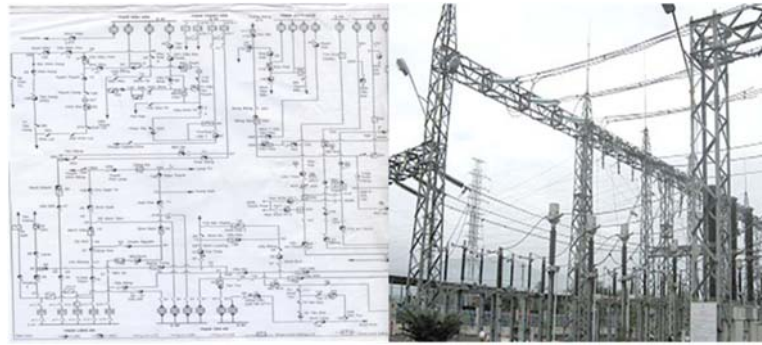


Figure 1. 110/22 kV Moc-Hoa substation, Vietnam.

2. RESISTIVE SFCL MODEL

Many models for SFCL have been developed such as resistive type, reactive type, transformer type, and hybrid type SFCLs [16]. In this study, we target practice the application of Resistive-SFCL. The sample of a Resistive-SFCL equipment is shown in Figure 2. And a corresponding MATLAB/Simulink based computer simulation is developed [17], using mathematical equations.

An impedance of SFCL with respect to time t is given by (1)-(4).

$$R_{SC}(t) = 0 \quad (t < t_0), \quad (1)$$

$$R_{SC}(t) = R_m \left[1 - \exp \left(-\frac{(t-t_0(\text{quench}))}{T_f(I_{\text{fault}})} \right) \right]^{\frac{1}{2}} \quad (t_0 \leq t < t_1), \quad (2)$$

$$R_{SC}(t) = \alpha_1(t - t_1) + \beta_1 \quad (t_1 \leq t < t_2), \quad (3)$$

$$R_{SC}(t) = \alpha_2(t - t_2) + \beta_2 \quad (t \geq t_2) \quad (4)$$



Figure 2. Example of Resistive SFCL device design, courtesy of Applied Superconductor [19].

Where $R_m=1\sim20\ (\Omega)$, $T_f=0.01$ and t_0 represents the convergence resistance, time constant and quench starting time, respectively. $\alpha_1=-80\ (\Omega/s)$, $\beta_1=R_m\ (\Omega)$ and t_1 represents the initial recovery slope, the recovery starting resistance, and recovery starting time, respectively. $\alpha_2=-160\ (\Omega/s)$, $\beta_2=R_m/2\ (\Omega)$ and t_2 represents the recovery slope, the second stage recovery starting resistance and recovery starting time, respectively. Quenching is the transition from the superconducting state to the current limiting state of SFCL start at $t_0=1\text{ sec}$. Four fundamental parameters are used for modeling resistive type SFCL. The parameters and their values are: 1) transition or response time = 2 msec, 2) minimum impedance = 0.01 Ohms and maximum impedance = 20 Ohms, 3) triggering current = 550 A and 4) recovery time = 10 msec [18], [19]. If passing current is larger than the triggering current level, the SFCL resistance increases its maximum value. When the current level falls below the triggering current level the system waits until the recovery time and then goes into normal state. Triggering current is the current flowing through the SFCL just before fault happened.

Figure 3 illustrates resistive SFCL model and the operating characteristics of R_SFCL using MATLAB/Simulink. When a recloser setup with the program is 2 Fast, 1 Delay (2F1D) and a fault current happened in power distribution system the impedance of SFCL will increase, and the recloser will be tripped, and SFCL will be recovered. The scheme is repeated two more times. The recovery time of SFCL must be setup to a valuable less than 500ms (According to the technical regulations of maximum time for fault clearance by electric equipment protection of power distribution system in Vietnam. Decision No: 32/2010/TT-BCT).

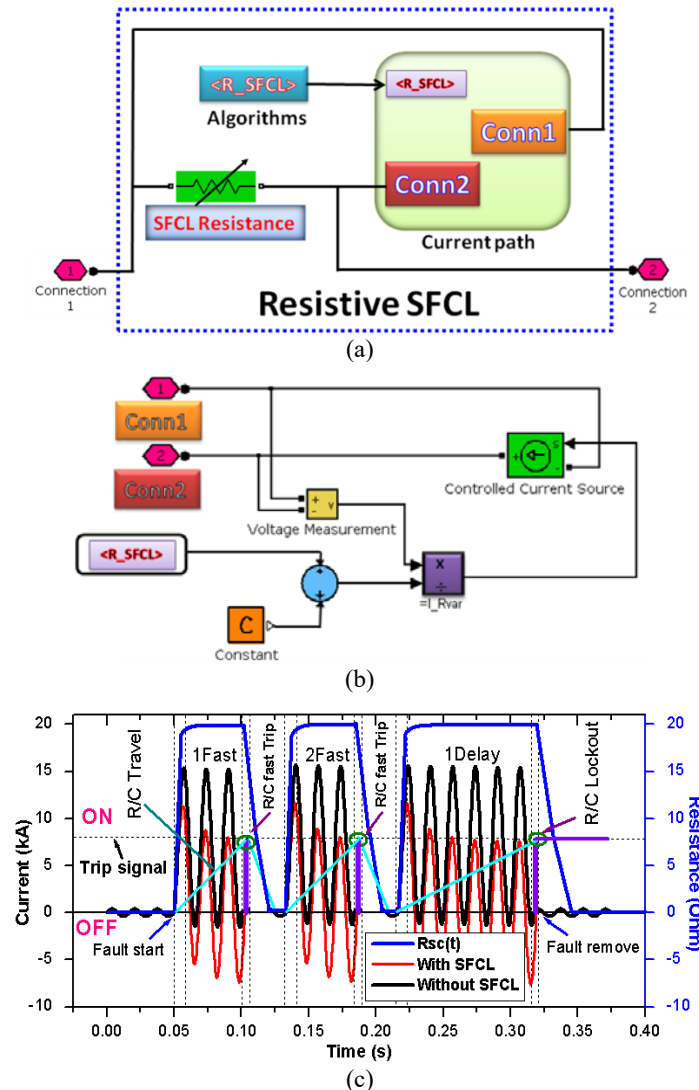


Figure 3. Resistive SFCL model and simulation results using Matlab/Simulink, a) Resistive type SFCL characteristics, b) SFCL model in Simulink, c) Operational characteristics of SFCL

3. CONFIGURATION OF DISTRIBUTION SYSTEM

Figure 4 shows a simplified diagram of a power distribution system using real data from Moc-Hoa substation, Vietnam. It consists of the two main transformers (MTr1, MTr2). Also, to protect MTr, feeders and load, various protective devices are installed, such as circuit breaker (CB), reclosers (R/C). And, in order to always operate the MTr in parallel, there is a switch (S/W) which connect MTr1 to MTr2, and this S/W is normally opened. The Distributed Generators (DGs) have applied to the power system at the load 2.

There is a SFCL installed at feeder of the power distribution system. Table 1 and Figure 5 represents the data of Figure 4.

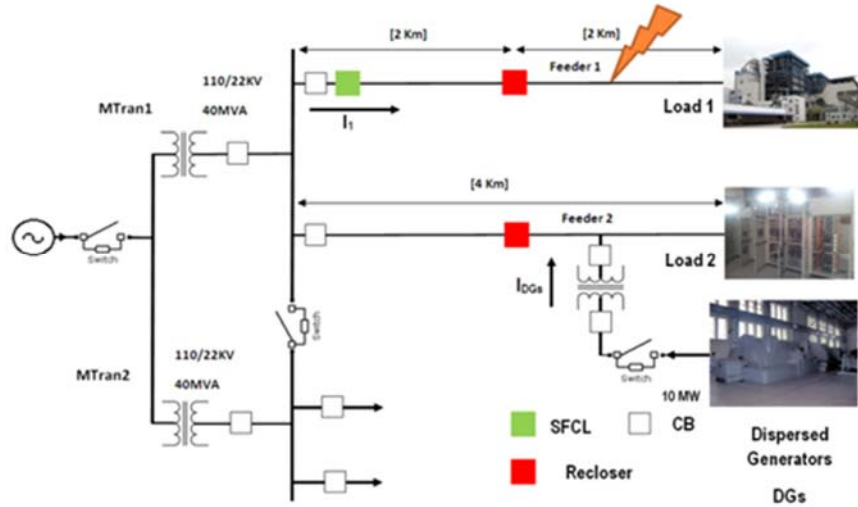


Figure 4. The single-line diagram of power distribution system

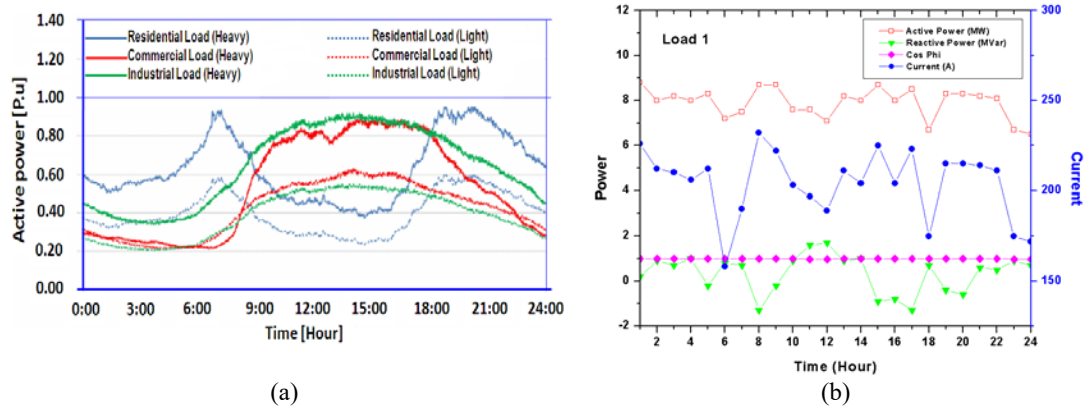


Figure 5. Example of load profiles and daily load curves, a) 24-hours load profiles of test feeder, b) Daily load curves using for simulation.

Table 1. The distribution system data

Circuit Parameters	Specifications
Utility	110 kV, 100 MVA, j1.78%
Main Transformer	110/22 kV, 40 MVA, j10%
Conductor impedance	$Z_L = 0.27 + j0.35 \Omega/\text{km}$
Feeder Length	4 km
Recloser Location	2 km from starting point
Distributed Generators (DGs)	22 kV/10 MVA

4. THE IMPACT OF SFCL ON VOLTAGE SAG IN DISTRIBUTION SYSTEM

Generally speaking, a voltage magnitude at bus of output terminal of MTr during fault can be represented as (5) if fault impedance is ignored [21].

$$V_{bus} = \frac{Z_L}{Z_{source} + Z_{Tr} + Z_L} \cdot V_{source} \quad (5)$$

Where Z_{source} , Z_{Tr} , and Z_L are source impedance, transformer impedance, and line impedance from source to fault location, respectively. While V_{source} is source voltage. The (5) also can approximately represent the voltage magnitude at all neighbor feeders. Different from (5), (6) and (7) are the voltage magnitude when SFCL is installed at two different locations: 1) At output terminal of main transformer or 2) starting point of each feeder.

$$V_{bus} = \frac{Z_L}{Z_{source} + Z_{Tr} + Z_{SFCL} + Z_L} \cdot V_{source} \quad (6)$$

$$V_{bus} = \frac{Z_L + Z_{SFCL}}{Z_{source} + Z_{Tr} + Z_{SFCL} + Z_L} \cdot V_{source} \quad (7)$$

where, Z_{SFCL} means the impedance being saturated at normal temperature.

5. STUDY CASES

To evaluate the effect of the SFCL in a distribution system with DGs, we used the MATLAB/Simulink software tool to model the components of the described system. We set the operation sequence of recloser to 2 fast – 1 delay (2F1D). If the fault current flows to the recloser and is bigger than the preset threshold value, the recloser is instantaneously tripped according to the time current characteristics curve which called fast operation (F). After several fast-trip operations of recloser, the recloser starts the delay operation (D). If the fault current is not removed after several fast trips and delay trips, the recloser would recognize the fault as a permanent fault and trip permanently. Such operation is called R/C lockout. The simulation were carried out with three phase short circuit created at 0.05s ($t=0.00s$ at beginning of the simulation). The total simulation time was 0.4s. The operation current during normal operation is 550A. Three different scenarios are considered in this paper:

5.1. Case 1: Without both SFCL and DGs:

The main purpose of this research is to discuss the fault current limiter and voltage sag without both SFCL and DGs, where the SFCL is installed at starting point and three-phase to ground short circuit can occur at feeder 1. Figure 6 shows current waveform at the fault point of feeder 1. As seen in Figure 6, the momentary peak short circuit current reached 66.75 kA.

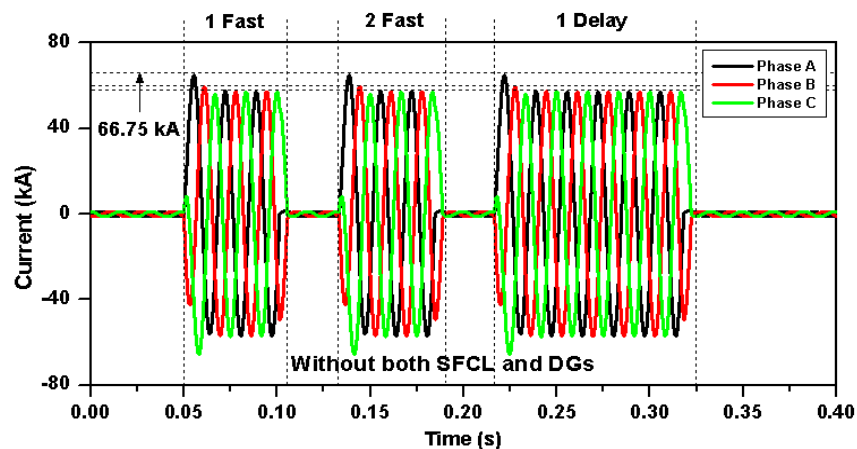


Figure 6. The current simulation results in fault current at feeder 1 with three phase short-circuit current without both SFCL and DGs at the fault point.

Figure 7 represent the short circuit of case 1 at the Bus, normal line (feeder 2). The maximum fault current is 42.14 kA.

As show in Figure 8, when a fault occurred at load side of feeder 1, the voltage become 0 (short interruption) at the fault point. Figure 9 illustrates the load voltage of feeder 2 at the normal line of case 1, where the voltage of feeder 2 has decreased to 10.22%.

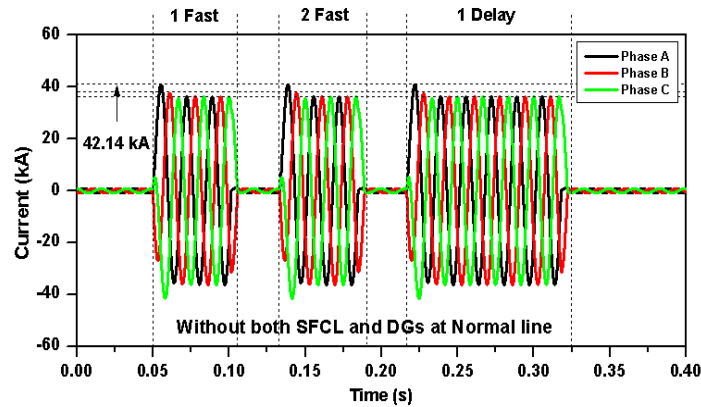


Figure 7. The current simulation results in fault current at feeder 1 with three phase short-circuit current without both SFCL and DGs at the normal line (feeder 2).

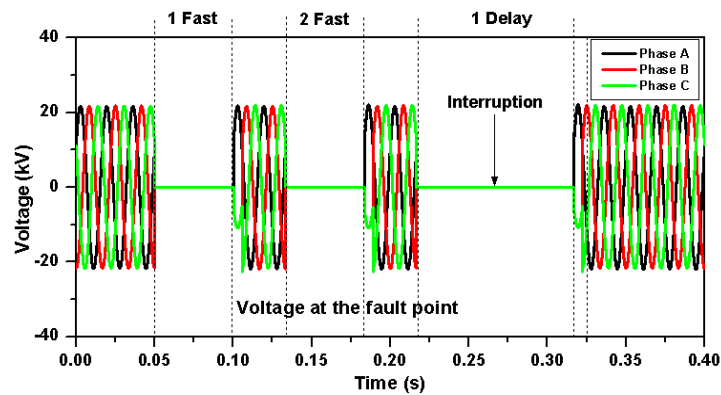


Figure 8. Voltage at the fault point

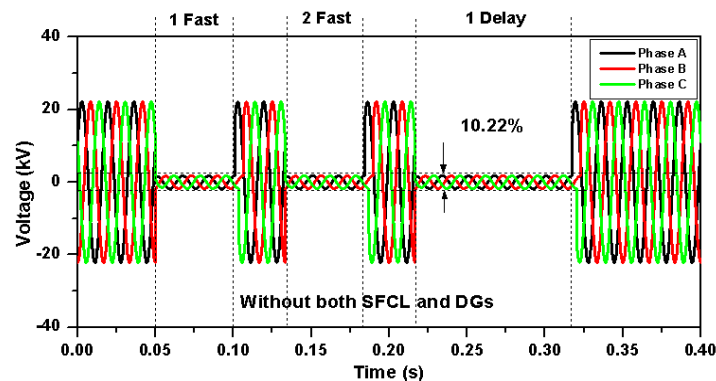


Figure 9. The load voltage simulation results on feeder 2 with three phase short circuit current without both SFCL and DGs at the normal line

5.2. Case 2: Without SFCL and with DGs:

The purpose of the study presented in this section is an analysis of the fault current limiter and voltage sag of case 2, where SFCL is installed at starting point (the same case1) and a fault occurred at feeder 1. Figure 10 presents the currents waveform at the fault point of case 2. The peak value of fault current is 88.18 kA. The short circuit current become large due to the flow from DGs. Figure 11 represent the short circuit of case 2 at the Bus, at the non-fault line (feeder 2). The maximum fault current is 63.17 kA. Figure 12 presents the voltage waveform of case 2. The voltage at feeder 2 has decreased to 12.97% during a fault.

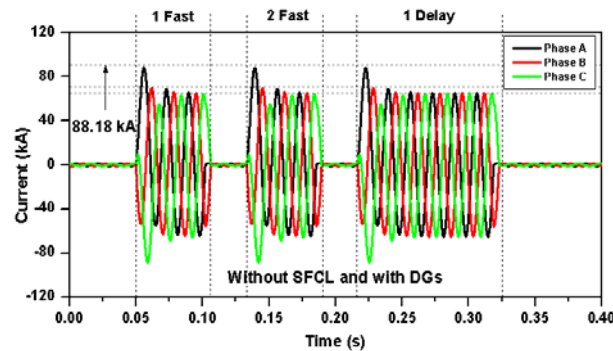


Figure 10. The current simulation results in fault at feeder 1 with three phase short-circuit current without SFCL and with DGs.

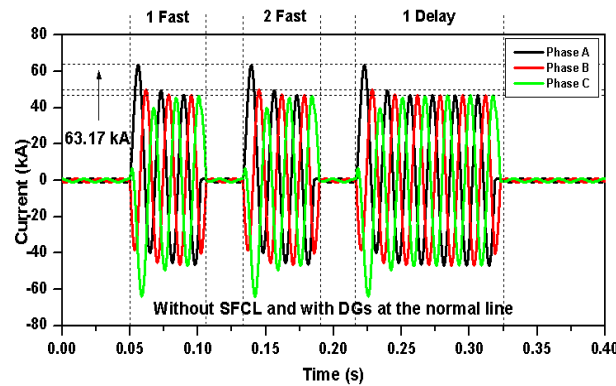


Figure 11. The simulation results in fault at feeder 1 with three phase short circuit current without SFCL and with DGs at the non-fault line (feeder 2).

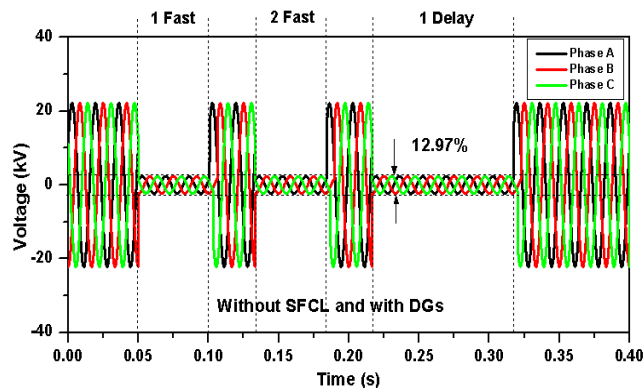


Figure 12. The load voltage simulation results in feeder 2 with three phase short circuit current without SFCL and with DGs.

5.3. Case 3: With SFCL and with DGs:

This case presents the fault current limiter and voltage drops for case 3, where SFCL installed at the starting point of feeder 1 and the short circuit is created at feeder 1. Figure 13 illustrates the current waveform at the fault point of case 3, when a fault occurred at feeder 1. As can be observed from Figure 13, with the installation of SFCL, the fault current is limited to the maximum value 39.12 kA by the resistance of the SFCL.

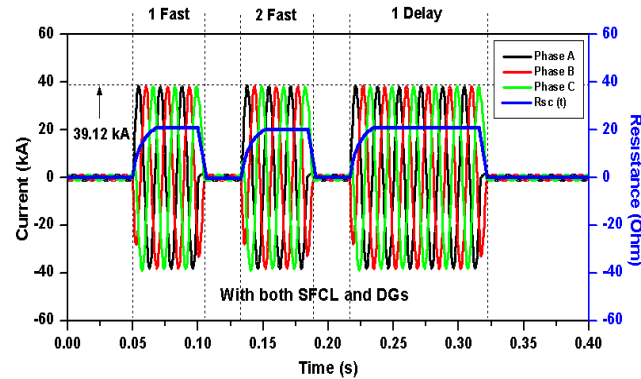


Figure 13. The current simulation results in fault at feeder 1 with three phase short circuit current with SFCL and with DGs at the fault point.

Figure 14 represent the short circuit of case 1 at the Bus, at the normal line (feeder 2). The maximum fault current is 24.17 kA. (According to the technical regulations, Decision No: 32/2010/TT-BCT of Short Circuit Current limit in Vietnam power distribution system, the maximum fault current should be less than 25 kA. If an SFCL was deployed at the starting point location which is the main route of the short circuit current, the maximum value of short circuit current could be limited to be 24.17 kA which is less than 25 kA and is within the switchgear rating.

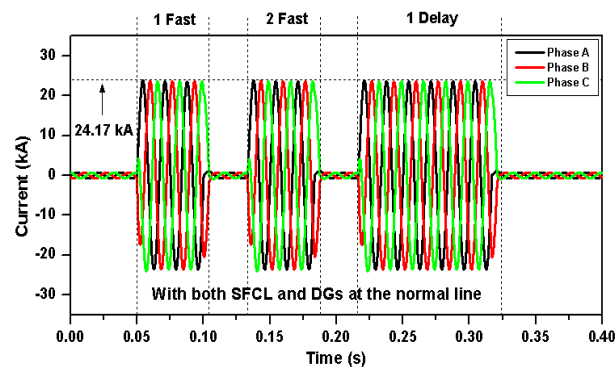


Figure 14. The current simulation results in fault at feeder 1 with three phase short circuit with SFCL and with DGs at the normal line (feeder 2).

Figure 15 shows the evaluation of three phase-to-ground voltage on the normal of feeder 1. With insertion SFCL, the Bus voltage level can get back to more than 93.95% of the normal level when the SFCL's limiting resistance is in the power distribution system.

Figure 16, Figure 17, Figure 18 and Figure 19 shows fault current, RMS current, voltage, RMS value of voltage magnitude at feeder 1 and feeder 2, respectively for three cases. When the SFCL is applied at feeder 1, the voltage sag improved due to the resistance of SFCL. Table 2 summarizes simulation results of current and voltage for three cases.

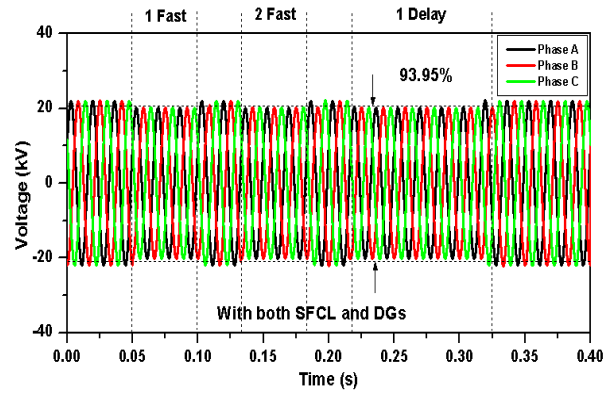


Figure 15. The load voltage simulation results in feeder 2 with three phase short circuit current without SFCL and with DGs.

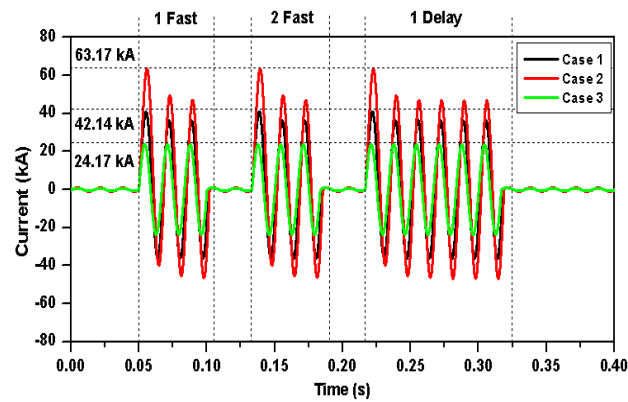


Figure 16. The current simulation results in fault on feeder 1 with three phase short circuit current for three cases.

Table 2. Summary of simulation results for three cases

No.	SC current at the fault point (kA)	SC current at the Bus (Normal line) (kA)	Voltage at the Bus (Normal line) (%)	Voltage at the fault point (kV)
Case 1	66.75	42.14	10.22	Short Interruption (0)
Case 2	88.15	63.17	12.97	Short Interruption (0)
Case 3	39.12	24.17	93.95	Short Interruption (0)

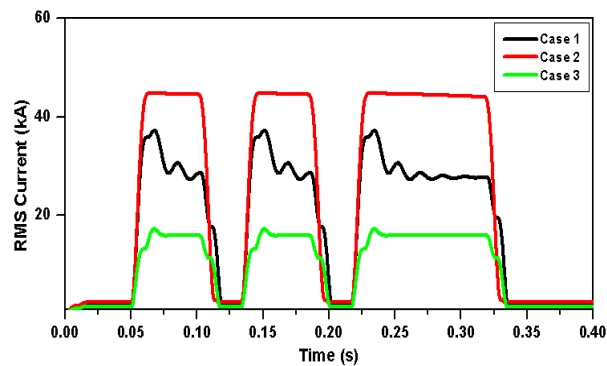


Figure 17. The simulation results of RMS current in fault at feeder 1 with three phase short circuit current for three cases.

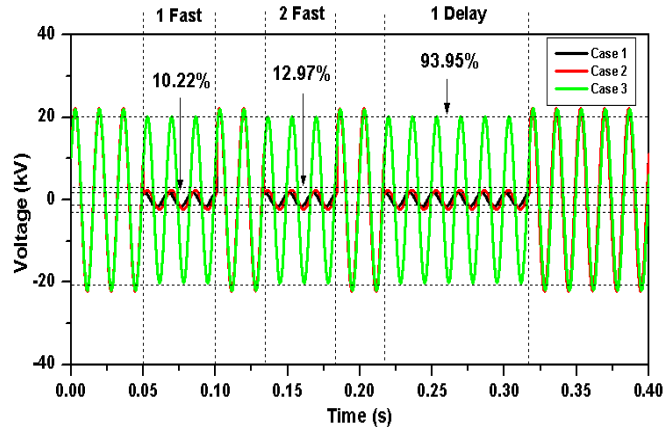


Figure 18. Simulation results of load voltage in feeder 2 with three phase short circuit for three cases.

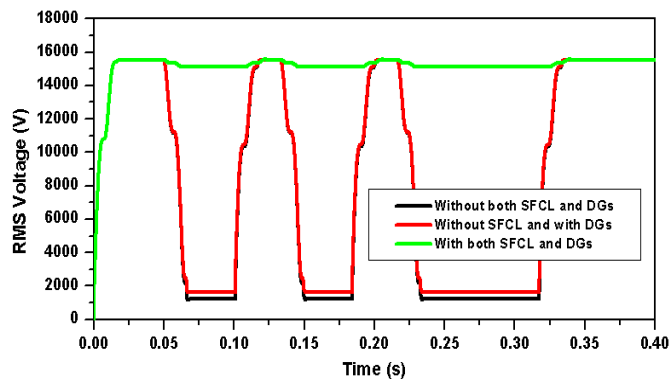


Figure 19. Simulation results of load RMS voltage in feeder 2 with three phase short circuit for three cases.

6. CONCLUSION

In this paper, we have analyzed and discussed the application of SFCL to the 22 kV distribution system with DGs in a southern Vietnam power system. The effectiveness of SFCL was evaluated by the simulation using Matlab/Simulink program. The results illustrate that the increase of the fault current with the introduction of DGs can be limited using SFCL. Thus, the DGs can be easily introduced to the power distribution system. Besides, we apply the SFCL to a 22 kV feeder at Moc-Hoa substation, Vietnam, to reduce the fault current and improve the severity of voltage sag. In the future, different types of fault and protective coordination will be also considered for the smart grid, and the effectiveness of SFCL will be validated.

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